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EXAMINER	
MCCARTNEY, LINZY T	
ART UNIT	**PAPER NUMBER**
2671	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/735,689	BENTZ, OLE	
	Examiner	Art Unit	
	Linzy McCartney	2671	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 May 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-7,9,11-15,17-22,24 and 26-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-7,9,11-15, 17-22, 24, 26-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 December 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 9, 2, 3, 5, 6, 17, 18, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,953,015 to Choi.

a. Referring to claim 9, Choi discloses calculating the square of the ratio between the number of texels for on pixel (column 3, lines 20-30), approximating a base-two logarithm of the square of the ratio (column 3, lines 50-55) and that the LOD is signed fixed point binary value (column 5, lines 65-67; column 6, lines 20-30). Choi does not explicitly disclose dividing the result by two to provide the LOD or that the LOD has an integer portion five bits in length. Choi discloses incorporating the ½ factor in the approximation (column 3, lines 50-55) and it is well known in the art to incorporate enough bits to specify a desired range of numbers, Official Notice taken. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the invention of Choi by dividing by two after approximating a base-two logarithm of the square of the ratio and to have the integer portion five bits in length. The suggestion/motivation for doing so would have been because it would allow a more exact approximation of the LOD and it would allow a greater number of LODs to be specified.

b. Referring to claim 2, Choi does not expressly disclose wherein dividing the result by two comprises shifting a binary value of the LOD right one-bit. However, Examiner takes Official Notice that shifting a binary value to the right one-bit to divide is conventional and well known. It would have been obvious at the time the invention was made to one of ordinary skill in the art to divide a binary number by two by shifting a binary value right one-bit since the Examiner takes Official Notice that dividing a binary number by two by shifting a binary value right one bit is well-known and conventional.

c. Referring to claim 3, Choi discloses calculating the square of a first ratio between the number of texels for one pixel along a first axis and the square of a second ration between the number of texels for one pixel along a second axis orthogonal to the first axis; and selecting the greater of the square of the first ration and the square of the second ratio for calculating the LOD (column 3, lines 45-50).

d. Referring to claim 5, Choi discloses wherein the square of the ratio comprises an unsigned fixed-point binary value having an integer portion and a fractional portion (column 5, lines 8-11).

e. Referring to claim 6, Choi does not explicitly disclose wherein the integer portion is 27 bits in length. As noted above, it is well known in the art to incorporate enough bits to specify a desired range of numbers, Official Notice taken.

f. Referring to claim 7, Choi suggests the fractional portion is 5 bits in length (column 5, lines 12-13).

g. Referring to claim 17, Choi does not expressly disclose a shifting circuit coupled to receive the result of the approximation and adapted to divide the approximation by two

by shifting the approximation right one-bit. However, Examiner takes Official Notice that utilizing a shifting circuit to shift a binary value to the right one-bit to divide is conventional and well known. It would have been obvious at the time the invention was made to one of ordinary skill in the art to divide a binary number by two by utilizing a shifting circuit to shift a binary value right one-bit since the Examiner takes Official Notice that dividing a binary number by two by utilizing a shifting circuit to shift a binary value right one bit is well-known and conventional.

h. Referring to claim 18, Choi discloses calculating the square of a first ratio between the number of texels for one pixel along a first axis and the square of a second ratio between the number of texels for one pixel along a second axis orthogonal to the first axis; and selecting the greater of the square of the first ration and the square of the second ratio for calculating the LOD (column 3, lines 55 – column 4, line 15).

i. Referring to claim 24, Choi discloses a means for calculating the square of the ratio between the number of texels applied to one pixel from the texel coordinates of a texture map and pixel coordinates for pixels of a graphics image (column 3, line 55- column 4, line, 15) and a means for approximating a base-two logarithm of the square of the ratio (column 3, line 55- column 4, line, 15). Choi does not explicitly disclose a means for dividing the result of the approximation by two to compute the LOD or wherein the integer portion is represented by five bits. As noted above, it would be obvious to modify the teachings of Choi to include circuitry to multiply the approximated logarithm by ½, instead of incorporating the ½ factor into the approximation and it is well

known in the art to incorporate enough bits to specify a desired range of numbers, Official Notice taken.

3. Claims 4, 15, 11-14, and 19-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Choi as applied to claims 9 and 15 above and further in view of National Semiconductor, "*Easy Logarithms for COP400*" (NS).

a. Referring to claim 4, Choi as applied to claim 9 meets the limitations recited in claim 4 except shifting the square of the ratio left by the number of leading zeros (LZs) and ignoring the most significant bit (MSB) of the resulting number to produce a first number; calculating a six-bit signed integer value from the equation: 6-bit signed integer = [(number of integer bits – 1) – LZs]; concatenating the six-bit signed integer value to a first number; and defining the five MSBs of the resulting number as the signed integer portion of the LOD. NS discloses shifting the square of a number left by the number of leading zeros and the MSB, effectively ignoring the MSB (page 1, column 2, paragraph 3); calculating a characteristic (integer) based on the number of characteristic bits minus the number of shifts required, effectively the [(number of integer bits – 1) – LZs] (page 1, column 2, paragraph 3); concatenating the integer value to first number (page 1, Figure 3); and defining the resulting number as the integer portion (page 1, column 2, paragraph 3 and Figure 3). At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the disclosure of Choi with the teachings of NS. The suggestion/motivation for doing so would have been to reduce the complexity and number of iterations in logarithm calculation (NS, page 1, paragraph 1) and produce a more accurate logarithm approximation.

b. Referring to claim 15, Choi discloses calculating the square of a first ratio between the number of texels for one pixel along a first axis and the square of a second ratio between the number of texels for one pixel along a second axis orthogonal to the first axis; selecting the greater of the square of the first ratio and the square of the second ratio for calculating the LOD (column 3, lines 45-50); the LOD has a fractional portion (column 5, lines 65-67; column 6, lines 20-30) and as noted in the rejection of claims 1 and 2 above, it would be obvious to multiply to the ½ factor disclosed by Choi (column 3, lines 50-55) after the logarithm approximation and it is well known to shift a binary number right one-bit to perform division. Choi does not explicitly disclose the integer portion of the LOD is five bits in length; shifting the selected square of the ratio left by the number of leading zeros (LZs) and ignoring the most significant bit (MSB) of the resulting number to produce a first number; calculating a six-bit signed integer value from the equation: 6-bit signed integer = [(number of integer bits – 1) – LZs], where the number of integer bits is the number of integer bits representing the selected square of the ratio; concatenating the six-bit signed integer value to a first number; defining the five MSBs of the resulting number as the signed integer portion of the LOD. As noted in the rejection of claim 4 above, NS discloses approximating a logarithm by shifting a number left by the number of leading zeros (LZs) and ignoring the most significant bit (MSB) of the resulting number to produce a first number (page 1, column 2, paragraph 3); calculating a six-bit signed integer value from the equation: 6-bit signed integer = [(number of integer bits – 1) – LZs] ((page 1, column 2, paragraph 3); concatenating the six-bit signed integer value to the first number (page 1, Figure 3) and defining the five

MSBs of the resulting number as a signed integer portion (page 1, column 2, paragraph 3 and Figure 3) As noted above, it is well known in the art to incorporate enough bits to specify a desired range of numbers, Official Notice taken. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the disclosure of Choi with the teachings of NS and wherein the integer portion is five bits in length. The suggestion/motivation for doing so would have been to reduce the complexity and number of iterations in logarithm calculation (NS, page 1, paragraph 1) and produce a more accurate logarithm approximation and because it would allow a greater number of LODs to be specified.

c. Referring to claim 11, Choi discloses the square of the ratio comprises an unsigned fixed-point binary value having an integer portion and a fractional portion (column 5, lines 8-11).

d. Referring to claim 12, Choi does not explicitly disclose wherein the integer portion is 27 bits in length. As noted above, it is well known in the art to incorporate enough bits to specify a desired range of numbers, Official Notice taken.

e. Referring to claim 13, Choi discloses wherein the fractional portion is 5 bits in length (column 5, lines 12-13).

f. Referring to claim 14, Choi discloses the LOD comprises a signed fixed point binary value having an integer portion and a fractional portion (column 6, lines 20-26).

g. Referring to claim 19, Choi as applied to claim 16 meets the limitations recited in claim 19 except shifting the square of the ratio left by the number of leading zeros (LZs) and ignoring the most significant bit (MSB) of the resulting number to produce a first

number; calculating a six-bit signed integer value from the equation: 6-bit signed integer = [(number of integer bits – 1) – LZs]; concatenating the six-bit signed integer value to a first number; and defining the five MSBs of the resulting number as the signed integer portion of the LOD. NS discloses shifting the square of a number left by the number of leading zeros and the MSB, effectively ignoring the MSB (page 1, column 2, paragraph 3); calculating a characteristic (integer) based on the number of characteristic bits minus the number of shifts required, effectively the [(number of integer bits – 1) – LZs] (page 1, column 2, paragraph 3); concatenating the integer value to first number (page 1, Figure 3); and defining the resulting number as the integer portion (page 1, column 2, paragraph 3 and Figure 3). At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the disclosure of Choi with the teachings of NS. The suggestion/motivation for doing so would have been to reduce the complexity and number of iterations in logarithm calculation (NS, page 1, paragraph 1) and produce a more accurate logarithm approximation.

h. Referring to claim 20, Choi discloses wherein the square of the ratio comprises an unsigned fixed-point binary value having an integer portion and a fractional portion (column 5, lines 8-11).

i. Referring to claim 21, Choi does not explicitly disclose wherein the integer portion is 27 bits in length. As noted above, it is well known in the art to incorporate enough bits to specify a desired range of numbers, Official Notice taken.

j. Referring to claim 22, Choi discloses wherein the fractional portion is 5 bits in length (column 5, lines 12-13).

4. Claims 26-28, 30, 32-37 and 39-43are rejected under 35 U.S.C. 103(a) as being unpatentable over Choi in view of U.S. Patent No. 6,292,191 to Vaswani et al. (Vaswani).

a. Referring to claim 26, Choi discloses a LOD computation circuit adapted to receive signals representing texel coordinates for texels of a texture map and pixel coordinates for pixels of a graphics image to calculate a level-of-detail (LOD) (column 3, lines 55-60 and Figure 2), the computation circuit calculating the square of the ratio between the number of texels applied to one pixel form the texel and pixel coordinates (column 3, line 60 – column 4, line 14), approximating a base-two logarithm of the square of the ratio (column 3, line 60 – column 4, line 14). Choi does not explicitly disclose a bus interface for coupling to a system bus; a graphics processor coupled to the bus interface to process graphics data; address and data busses coupled to the graphics processor to transfer address and graphics data to and from the graphics processor; display logic coupled to the data bus to drive a display; or dividing the approximation by two to compute the LOD. As noted above, it would be obvious to modify the teachings of Choi to include circuitry to multiply the approximated logarithm by ½, instead of incorporating the ½ factor into the approximation. Vaswani discloses a bus interface for coupling to a system bus (Figure 3); a graphics processor coupled to the bus interface to process graphics data (Figure 3); address and data busses coupled to the graphics processor to transfer address and graphics data to and from the graphics processor (Figure 3); display logic coupled to data bus to drive a display (Figure 3). At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to

modify the disclosure of Choi with the teachings of Vaswani. The suggestion/motivation for doing so would have been to process and display the graphic data.

b. Referring to claim 27, Choi does not explicitly disclose a shifting circuit adapted to divide by two by shifting the approximation right one-bit. However, Examiner takes Official Notice that utilizing a shifting circuit to shift a binary value to the right one-bit to divide is conventional and well known. It would have been obvious at the time the invention was made to one of ordinary skill in the art to divide a binary number by two by utilizing a shifting circuit to shift a binary value right one-bit since the Examiner takes Official Notice that dividing a binary number by two by utilizing a shifting circuit to shift a binary value right one bit is well-known and conventional.

c. Referring to claim 28, Choi discloses calculating the square of a first ratio between the number or texels for one pixel along a first axis and the square of a second ratio between the number of texels for one pixel along a second axis orthogonal to the first axis; and selecting the greater of the square of the first ration and the square of the second ratio for calculating the LOD (column 3, lines 45-50).

d. Referring to claim 30, Choi discloses the square of the ratio calculated by the LOD computation circuit comprises an unsigned fixed-point binary value having an integer portion and a fractional portion (column 5, lines 8-11).

e. Referring to claim 31, Choi does not explicitly disclose wherein the integer portion is 27 bits in length. As noted above, it is well known in the art to incorporate enough bits to specify a desired range of numbers, Official Notice taken.

f. Referring to claim 32, Choi suggests the fractional portion is 5 bits in length (column 5, lines 12-13).

f. Referring to claim 33, Choi discloses the LOD computed by the LOD computation circuit comprises a signed fixed point binary value having an integer portion and a fractional portion (column 6, lines 20-26).

g. Referring to claim 34, Choi does not explicitly disclose wherein the integer portion is 5 bits in length. As noted above, it is well known in the art to incorporate enough bits to specify a desired range of numbers, Official Notice taken.

g. Referring to claim 35, Choi discloses a LOD computation circuit adapted to receive signals representing texel coordinates for texels of a texture map and pixel coordinates for pixels of a graphics image to calculate a level-of-detail (LOD) (column 3, lines 55-60 and Figure 2), the computation circuit calculating the square of the ratio between the number of texels applied to one pixel form the texel and pixel coordinates (column 3, line 60 – column 4, line 14), approximating a base-two logarithm of the square of the ratio (column 3, line 60 – column 4, line 14). Choi does not explicitly disclose a system processor; a system bus coupled to the system processor; a system memory coupled to the system bus; and a graphics processing system coupled to the system bus, the graphics processing system comprising: a bus interface for coupling to a system bus; a graphics processor coupled to the bus interface to process graphics data; address and data busses coupled to the graphics processor to transfer address and graphics data to and from the graphics processor; display logic coupled to the data bus to drive a display; or dividing the result of the approximation by two to compute the LOD.

As noted above, it would be obvious to modify the teachings of Choi to include circuitry to multiply the approximated logarithm by ½, instead of incorporating the ½ factor into the approximation. Vaswani discloses a bus interface for coupling to a system bus (Figure 3); a graphics processor coupled to the bus interface to process graphics data (Figure 3); address and data busses coupled to the graphics processor to transfer address and graphics data to and from the graphics processor (Figure 3); display logic coupled to data bus to drive a display (Figure 3). At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the disclosure of Choi with the teachings of Vaswani. The suggestion/motivation for doing so would have been to process and display the graphic data.

h. Referring to claim 36, Choi does not expressly disclose a shifting circuit coupled to receive the result of the approximation and adapted to divide the approximation by two by shifting the approximation right one-bit. However, Examiner takes Official Notice that utilizing a shifting circuit to shift a binary value to the right one-bit to divide is conventional and well known. It would have been obvious at the time the invention was made to one of ordinary skill in the art to divide a binary number by two by utilizing a shifting circuit to shift a binary value right one-bit since the Examiner takes Official Notice that dividing a binary number by two by utilizing a shifting circuit to shift a binary value right one bit is well-known and conventional.

i. Referring to claim 37, Choi discloses calculating the square of a first ratio between the number of texels for one pixel along a first axis and the square of a second ration between the number of texels for one pixel along a second axis orthogonal to the

first axis; and selecting the greater of the square of the first ration and the square of the second ratio for calculating the LOD (column 3, lines 55 – column 4, line 15).

j. Referring to claim 39, Choi discloses the square of the ratio calculated by the LOD computation circuit comprises an unsigned fixed-point binary value having an integer portion and a fractional portion (column 5, lines 8-11).

k. Referring to claim 40, Choi does not explicitly disclose wherein the integer portion is 27 bits in length. As noted above, it is well known in the art to incorporate enough bits to specify a desired range of numbers, Official Notice taken.

k. Referring to claim 41, Choi discloses wherein the fractional portion is 5 bits in length (column 5, lines 12-13).

l. Referring to claim 42, Choi discloses the LOD computed by the LOD computation circuit comprises a signed fixed point binary value having an integer portion and a fractional portion (column 6, lines 20-26).

m. Referring to claim 43, Choi does not explicitly disclose wherein the integer portion is 5 bits in length. As noted above, it is well known in the art to incorporate enough bits to specify a desired range of numbers, Official Notice taken.

5. Claims 29 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Choi in view of Vaswani as applied to claims 26 and 35 above and further in view of NS.

a. Referring to claim 29, the modified method of Choi as applied to claim 26 above meets the limitations recited in claim 29, except shifting the square of the ratio left by the number of leading zeros (LZs) and ignoring the most significant bit (MSB) of the resulting number to produce a first number; calculating a six-bit signed integer value

from the equation: 6-bit signed integer = [(number of integer bits – 1) – LZs]; concatenating the six-bit signed integer value to a first number; and defining the five MSBs of the resulting number as the signed integer portion of the LOD. NS discloses shifting the square of a number left by the number of leading zeros and the MSB, effectively ignoring the MSB (page 1, column 2, paragraph 3); calculating a characteristic (integer) based on the number of characteristic bits minus the number of shifts required, effectively the [(number of integer bits – 1) – LZs] (page 1, column 2, paragraph 3); concatenating the integer value to first number (page 1, Figure 3); and defining the resulting number as the integer portion (page 1, column 2, paragraph 3 and Figure 3). At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the disclosure of Choi with the teachings of NS. The suggestion/motivation for doing so would have been to reduce the complexity and number of iterations in logarithm calculation (NS, page 1, paragraph 1) and produce a more accurate logarithm approximation.

b. Referring to claim 38, the modified method of Choi as applied to claim 35 above meets the limitations recited in claim 38, except shifting the square of the ratio left by the number of leading zeros (LZs) and ignoring the most significant bit (MSB) of the resulting number to produce a first number; calculating a six-bit signed integer value from the equation: 6-bit signed integer = [(number of integer bits – 1) – LZs]; concatenating the six-bit signed integer value to a first number; and defining the five MSBs of the resulting number as the signed integer portion of the LOD. NS discloses shifting the square of a number left by the number of leading zeros and the MSB,

effectively ignoring the MSB (page 1, column 2, paragraph 3); calculating a characteristic (integer) based on the number of characteristic bits minus the number of shifts required, effectively the [(number of integer bits – 1) – LZs] (page 1, column 2, paragraph 3); concatenating the integer value to first number (page 1, Figure 3); and defining the resulting number as the integer portion (page 1, column 2, paragraph 3 and Figure 3). At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the disclosure of Choi with the teachings of NS. The suggestion/motivation for doing so would have been to reduce the complexity and number of iterations in logarithm calculation (NS, page 1, paragraph 1) and produce a more accurate logarithm approximation.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Linzy McCartney** whose telephone number is **(703) 605-0745**. The examiner can normally be reached on Mon-Friday (8:00AM-5: 30PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Mark Zimmerman**, can be reached at **(703) 305-9798**.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

ltm
12 December 2003

MARK ZIMMERMAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600